Course Syllabus

Hardware Description Languages

Objective:
The goal of the course is to study hardware description languages and describe their role in the electronic design automation environment. The course also focuses on Verilog basics and VHDL basics.

Class Hours:
The course duration is 50 hours, lectures volume is 40 hours, and laboratory works are 10 hours.

Reference Materials:
To study the course the necessary list of references is given below.

1. V. Pedroni. Finite State Machines in Hardware: Theory and Design (with VHDL and SystemVerilog). The MIT Press; 2013
2. C. Kloos, E. Cerny. Hardware Description Languages and their Applications: Specification, modelling, verification and synthesis of microelectronic systems. Springer; 2013
3. Ch. Spear, G. Tumbush. SystemVerilog for Verification: A Guide to Learning the Testbench Language Features. Springer; 3rd edition, 2012
4. M. Ferdjallah. Introduction to Digital Systems: Modeling, Synthesis, and Simulation Using VHDL, Wiley; 1st edition, 2011
5. M. Ciletti. Advanced Digital Design with the Verilog HDL. Prentice Hall; 2nd edition, 2010
6. M. Mano, C. Ciletti. Digital Design: With an Introduction to the Verilog HDL. Prentice Hall; 5th edition, 2012

Lectures (50 hours):

The role and Classification of HDLs (2 hours)

- The role of HDLs in state-of-the-art methodologies of digital systems design. Multi-level approach to digital systems design.
  The design flow of digital systems. Synthesis of digital systems. The digital standard cell libraries. Design verification of digital systems. Simulation of digital systems. Overview of HDLs. Design of digital systems using HDLs.

Verilog (18 hours)

- Modeling concepts. Levels of abstraction. Design methodologies. Basic concepts. Module, module header format. Lexical conventions: comments, identifiers, numbers, strings. Data types: nets, registers, vectors, arrays. Parameter types. Operators. Operator types, precedence. Sequential and parallel blocks. Comparison of sequential and parallel blocks. Basic compiler directives. Behavioral modeling. Behavioral modeling blocks: always block, event-based timing control, branch statements, case, casex, casez. Procedural assignments: blocking and non-blocking. Data flow modeling. Assign statements. Delays. Implicit net declaration. Regular, implicit continuous assignment and net declaration delay. Logic statement implementation. The conditional operator.
  Gate level modeling. Gate types: and/or, buf/not gates, bufif/notif gates. Gate truth tables. Gate delays. Specify block. UDP. Ports. Port connection rules: by order and name.
  Switch level modeling. Primitives. Use of trireg. Testbench creation. Initial block. Delay-based timing control. System tasks. Monitoring a simulation.
  Looping constructs: while loop, for loop, repeat, forever loop. VCS simulation examples. VCD file fragment. Tasks and functions. Differences between tasks and functions.

VHDL (30 hours)

- VHDL's history. Benefits of VHDL. Concepts of VHDL. Entity and Architecture. Behavioral, data flow and structural specifications. Mixed structural-behavioral models. Syntax of VHDL.
  Basic elements of VHDL. Timing model. Delay types: delta, transport and inertial delays. Data types. Scalar data types: numerical, physical (operations with physical types, time description), enumerated. Attributes of scalar data types. Conversion of scalar data types. Subtypes.

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Embedded subtypes. Composite data types. Arrays. Definition of initial values. Attributes of array data type. Arrays of unlimited length. Operations with arrays. Fragments of arrays. Type conversion. Records. Data type access. Assignment of access. Description of access data type. Access to arrays. Abstract data types.
Description of constants, variables, signals. Files. Statements. Concurrent and sequential statements. Assignment statement. Packages and libraries. Attributes. VHDL Operators. Example code.